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SILICON VALLEY PATENT GROUP LLP 2350 MISSION COLLEGE BOULEVARD SUITE 360 SANTA CLARA, CA 95054				
			EXAMINER LAROSE, COLIN M	
			ART UNIT 2627	PAPER NUMBER

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/974,721

Applicant(s)

ZHOU ET AL.

Examiner

Colin M. LaRose

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 and 22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-16 is/are allowed.
- 6) ☒ Claim(s) 1-3, 7, 8 and 22 is/are rejected.
- 7) ☒ Claim(s) 4-6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Arguments and Amendments***

1. Applicant's amendments and arguments filed 24 August 2005, have been entered and made of record.

### ***Claim Objections***

2. In view of Applicant's amendment to claim 9, the previous claim objection has been withdrawn.

### ***Response to Arguments***

3. Applicant's arguments with respect to the rejection of claim 1 in view of Hennessey have been considered and are persuasive. Accordingly, the rejection has been withdrawn. However, Hennessey is still believed to anticipate claim 1. Examiner relies upon figures 9-12 of Hennessey below (rather than figure 4) in a new ground of rejection.

Regarding claim 22, Examiner believes that figures 9-12 better teach the claimed invention. Therefore, these figures are relied upon below for the rejection of claim 22.

4. Applicant's arguments with respect to claim 1 in view of Michael have been considered but are not persuasive. Applicant argues that Michael does not disclose "learning a second pattern at the de-skew site on a second wafer layer," as claimed. In the previous Office action, Examiner interpreted the learned 1-D feature image obtained in figure 14 as corresponding to the claimed "second pattern ... on a second wafer layer." It is respectfully submitted that such an

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interpretation is valid. Figure 14 shows the run-time steps of learning a feature pattern, which is to be compared to a previously learned training image during train-time at step 158. The 1-D feature image learned at step 156 is the second pattern contained in a wafer layer and is to be compared to the 1-D feature image of the good sample contained in a different layer that has been learned via the process in figure 11. The two 1-D feature images learned in the processes of figures 11 and 14 are not contained in the same layer, therefore, the 1-D feature image learned in figure 14 is considered to be on a "second wafer layer."

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,696,835 by Hennessey et al. ("Hennessey").

Regarding claim 1, Hennessey discloses a method (figures 9-12) for forming a recipe for de-skewing wafers, comprising:

learning a first pattern at a de-skew site on a first wafer layer (step 174, figure 11: method learns a first target pattern on a first layer via conversion to a first target primitive);

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saving the first pattern and its location in a recipe for de-skewing wafers (i.e. the first target primitive and its designated location are somehow saved so that they can later be utilized for comparison to a second target primitive at step 176 – see e.g. figure 12);

learning a second pattern at the de-skew site on a second wafer layer (step 174, figure 11: method learns a second target pattern on a second layer via conversion to a second target primitive); and

saving the second pattern in the same recipe for de-skewing wafers (i.e. the second target primitive and its designated location are somehow saved so that they can later be utilized for comparison to the first target primitive at step 176 – see e.g. figure 12).

Regarding claim 22, Hennessey discloses a method (figure 9-12) for forming a recipe for de-skewing wafers, comprising:

learning a first pattern at a de-skew site on a first wafer layer (step 174, figure 11: method learns a first target pattern on a first layer via conversion to a first target primitive);

saving the pattern in the recipe for a plurality of wafer layers (i.e. the first target primitive and its designated location are somehow saved so that they can later be utilized for comparison to a second target primitive at step 176 – see e.g. figure 12);

determining if the first pattern matches a second pattern at the de-skew site on a second wafer layer (step 176, figure 11: the displacement between the target primitives is determined);  
and

using said first pattern to de-skew the first and second wafer layers when the first pattern matches the second pattern (i.e. the measure of the relative displacement between the two target primitives is used to de-skew the two layers – see col. 10/13-20).

7. Claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent 6,240,218 by Michael et al. (“Michael”).

Regarding claim 1, Michael discloses a method (figures 11 and 14) for forming a recipe for de-skewing wafers, comprising:

learning a first pattern at a de-skew site on a first wafer layer (figure 11 details the process of learning a template pattern on a wafer to generate a 1-D template image; the template pattern is a “good” sample located at a de-skew site (i.e. an area containing a fiducial mark) in a wafer layer, and learning the template pattern comprises generating a 1-D projection thereof – see e.g. column 7, lines 6-13);

saving the first pattern and its location in a recipe for de-skewing wafers (i.e. the projection of the template pattern is somehow saved so that it can later be utilized during the run-time phase for comparison to a 1-D feature image at step 158, figure 14; included with the projection of the template pattern is information regarding its location, or origin – see column 7, lines 14-25);

learning a second pattern at the de-skew site on a second wafer layer (figure 14 details the process of learning a feature pattern on a wafer to generate a 1-D feature image at step 156; the feature pattern is located at the de-skew site in a different wafer layer, such as any of the

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subsequent layers depicted in figure 1, and learning the feature pattern comprises generating a 1-D projection thereof – see e.g. column 8, lines 30-37); and

\ saving the second pattern in the same recipe for de-skewing wafers (i.e. the projection of the reference pattern is somehow saved so that it can later be utilized for comparison to the 1-D template image at step 158, figure 14).

It should be noted that Michael does not expressly disclose saving the first and second pattern in a physical medium, such as a memory or the like, however, the claim does not require this. Implicit in Michael's disclosure is that once the projections of the first and second patterns are learned, or extracted, they are retained so that they can be compared to each other. Since the information pertaining to neither pattern is discarded prior to comparison, both learned patterns are both considered to have been "saved," in accordance with the claim language.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 2, 3, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,240,218 by Michael et al. ("Michael") in view of U.S. Patent 6,240,208 by Garakani et al. ("Garakani").

Regarding claim 2, Michael does not disclose learning the first pattern comprises determining a score of uniqueness for the first pattern.

Garakani discloses a method for identifying reference patterns to be utilized for aligning wafers. In particular, Garakani discloses that it is advantageous to select reference patterns that are unique. Garakani teaches determining the uniqueness of potential reference patterns, and selecting from among the reference patterns on the basis of their uniqueness scores. For example, in figure 2, the uniqueness of various reference patterns is measured at step 240, and the suggested reference patterns are ordered at step 260 based in part on the uniqueness scores.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Michael by Garakani to determine a score of uniqueness for the first pattern to be learned, since Garakani discloses that it is advantageous to select a reference pattern utilized for aligning semiconductor wafer layers that is unique, and determining a score of uniqueness indicates whether a pattern to be learned is unique (see e.g. column 1, lines 19-32; column 6, lines 58-67).

Regarding claim 3, Garakani discloses selecting a first pattern that has a parameter value (e.g. uniqueness) greater than a threshold (see column 7, lines 51-59). Therefore, that pattern that is learned and saved according to Michael's teachings is sufficiently unique.

Regarding claim 7, Michael discloses learning the first pattern comprises removing a feature of the first pattern (column 7, lines 25-30: “confusing information” within the pattern is deleted).

However, Michael does not disclose determining a score of uniqueness for the first pattern without the feature, and then saving the pattern without the feature when the uniqueness score exceeds a threshold, as claimed.

Garakani discloses a method for identifying reference patterns to be utilized for aligning wafers. In particular, Garakani discloses that it is advantageous to select reference patterns that are unique. Garakani teaches determining the uniqueness of potential reference patterns, and selecting from among the reference patterns on the basis of their uniqueness scores. For example, in figure 2, the uniqueness of various reference patterns is measured at step 240, and the suggested reference patterns are ordered at step 260 based in part on the uniqueness scores.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Michael by Garakani to determine a score of uniqueness for the first pattern to be learned, since Garakani discloses that it is advantageous to select a reference pattern utilized for aligning semiconductor wafer layers that is unique, and determining a score of uniqueness indicates whether a pattern to be learned is unique (see e.g. column 1, lines 19-32; column 6, lines 58-67). Furthermore, it would have been obvious to compute the uniqueness score of the pattern and save the pattern with portions thereof deleted, since Michael teaches that it is advantageous to remove extraneous features within the pattern that do not relate to the salient features and are simply “confusing” (Michael, column 7, lines 25-30).

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11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,240,218 by Michael et al. ("Michael"), as applied to claim 1 above, in view of U.S. Patent 6,681,151 by Weinzimmer et al. ("Weinzimmer").

Regarding claim 8, Michael does not disclose that saving the first pattern in the recipe comprises saving a file name of a file including the first pattern. However, at the time of the invention, it was well-known in the art to store captured image data into image files. More particularly, Weinzimmer shows that it was obvious to store extracted fiducial patterns into data files for later use (see column 10, lines 35-53). Such a method of saving extracted fiducial data in a file is advantageous in that the file is easily accessible for future and/or repeated use.

#### *Allowable Subject Matter*

12. Regarding claim 9, Michael discloses the learning and saving steps, as noted above for claim 1. However, Michael does not appear to disclose the step of "dividing," as claimed.

Michael's disclosure focuses on the problem that patterns to be detected in subsequent wafer layers (cf. figure 18) may be degraded to point where they are indistinguishable from background. See column 1, lines 33-52.

Michael's disclosure proposes a solution to this problem and is illustrated in figure 7. In figure 7A, a 1-D projection of a "good" pattern consists of three discernible spikes. Figure 7B shows a degraded pattern to be matched to the good pattern. Two of the degraded pattern's spikes have been attenuated, while the third spike is missing (i.e. indistinguishable from background noise). Michael's system is able to recognize the degraded pattern even though it contains missing features.

Claim 9 seeks to remedy the same problem but does so in a different way. Michael does not disclose “dividing additional wafer layers into a plurality of layers where the de-skew site can be recognized using the first pattern and at least one wafer layer where the de-skew site cannot be recognized using said pattern.” In contrast, Michael does not divide out layers whose patterns are substantially degraded to the point that they cannot be recognized, because Michael teaches that they can be recognized using a 1-D projection even when they are severely degraded. Since Michael purports that all of the degraded patterns can be recognized, there is no disclosure of separating layers where the de-skew site can be recognized from those in which it cannot be recognized.

In addition, Michael does not disclose the learning and saving of an additional pattern for recognition of the “cannot be recognized” pattern(s), since none of Michael’s de-skew site are unable to be recognized.

For these reasons, claims 9-16 are allowable.

13. Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 4, neither Hennessey nor Michael fairly discloses or suggests comparing the first pattern and the second pattern before said learning the second pattern. In both Hennessey and Michael, the patterns are compared after both patterns have been learned.


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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (571) 272-7423. If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Bhavesh Mehta, can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600 Customer Service Office whose telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CML  
Group Art Unit 2627  
12 December 2005



**VIKKRAM BALI**  
**PRIMARY EXAMINER**